IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
MARIAUD ET AL.

Serial No. **Not yet assigned**

Filing Date: **Herewith**

For: **APPARATUS AND METHOD FOR ROCESSING INTERRUPTIONS IN A DATA TRANSMISSION OVER A BUS**

I HEREBY CERTIFY THIS PAPER OR FEE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED BELOW AND IS ADDRESSED TO: U.S. PATENT AND TRADEMARK OFFICE, P.O. BOX 2327, ARLINGTON, VA 22202.

EXPRESS MAIL NO: EL 768139885 US

DATE OF DEPOSIT: November 20, 2001

NAME: REGAN SAMPSON

SIGNATURE: Regan Sampson

10032147 .112601

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Claims:

Please cancel Claims 1 to 4.

Please add new Claims 5 to 22.

5. A computer system comprising:

a master apparatus; and

a slave apparatus for communicating with said master apparatus and communicating via the universal serial bus (USB) protocol, said slave apparatus comprising

a sending/receiving circuit for sending and receiving binary information to and from said master apparatus and supplying status signals based thereon,

a plurality of state latches and control circuitry cooperating therewith for receiving the status signals from said sending/receiving circuit and supplying state signals of said sending/receiving circuit based thereon,

a microprocessor for processing applications of said slave apparatus and also for processing the binary information received by said sending/receiving circuit, and

an interruption state latch and a control circuit cooperating therewith for supplying an interruption signal when said sending/receiving circuit has received the start of a new message after the start of the new message has been acknowledged and recorded by said sending/receiving circuit.

6. The computer system of Claim 5 wherein said control circuit for controlling said interruption state latch comprises at least one logic circuit for receiving the status signals from said sending/receiving circuit and setting said interruption state latch to a predetermined logic level to indicate a microprocessor interruption request.

7. The computer system of Claim 5 wherein said control circuitry for controlling said state latches prevents the binary information from said microprocessor from being written into said plurality of state latches during receipt of the start of the new message and during the presence of the interruption signal.

8. The computer system of Claim 5 wherein said master apparatus comprises a central processing unit.

9. The computer system of Claim 5 wherein said slave apparatus comprises a computer peripheral device.

10. The computer system of Claim 5 further comprising a cable connecting said master apparatus and said slave apparatus.

11. A computer system comprising:

a master apparatus; and

a slave apparatus for communicating with said master apparatus and comprising

a sending/receiving circuit for sending and receiving binary information to and from said master apparatus and supplying status signals based thereon,

a plurality of state latches and control circuitry cooperating therewith for receiving the status signals from said sending/receiving circuit and supplying state signals of said sending/receiving circuit based thereon,

a microprocessor for processing applications of said slave apparatus and also for processing the binary information received by said sending/receiving circuit, and

an interruption state latch for supplying an interruption signal when said sending/receiving circuit has received the start of a new message after the start of the new message has been

acknowledged and recorded by said sending/receiving circuit,

said control circuitry for controlling said state latches preventing the binary information from said microprocessor from being written into said plurality of state latches during receipt of the start of the new message and during the presence of the interruption signal.

12. The computer system of Claim 11 wherein said master apparatus and said slave apparatus communicate via the universal serial bus (USB) protocol.

13. The computer system of Claim 11 further comprising at least one logic circuit for receiving the status signals from said sending/receiving circuit and setting said interruption state latch to a predetermined logic level to indicate a microprocessor interruption request.

14. The computer system of Claim 11 wherein said master apparatus comprises a central processing unit.

15. The computer system of Claim 11 wherein said slave apparatus comprises a computer peripheral.

16. The computer system of Claim 11 further comprising a cable connecting said master apparatus and said slave apparatus.

17. A slave apparatus for communicating with a master apparatus via the universal serial bus (USB) protocol, said slave apparatus comprising:

a sending/receiving circuit for sending and receiving binary information to and from the master apparatus and supplying status signals based thereon;

a plurality of state latches and control circuitry cooperating therewith for receiving the status signals from said sending/receiving circuit and supplying state signals of said sending/receiving circuit based thereon;

a microprocessor for processing applications of the slave apparatus and also for processing the binary information received by said sending/receiving circuit; and

an interruption state latch and a control circuit cooperating therewith for supplying an interruption signal when said sending/receiving circuit has received the start of a new message after the start of the new message has been acknowledged and recorded by said sending/receiving circuit.

18. The slave apparatus of Claim 17 wherein said control circuit for controlling said interruption state latch comprises at least one logic circuit for receiving the status signals from said sending/receiving circuit and setting said interruption state latch to a predetermined logic level to indicate a microprocessor interruption request.

19. The slave apparatus of Claim 17 wherein said control circuitry for controlling said state latches prevents the binary information from said microprocessor from being written into said plurality of state latches during receipt of the start of the new message and during the presence of the interruption signal.

20. A method of processing interruptions in a slave apparatus for communicating with a master apparatus via the universal serial bus (USB) protocol, the method comprising:

sending and receiving binary information to and from the master apparatus via a sending/receiving circuit and supplying status signals based thereon;

generating state signals of the sending/receiving circuit based upon the status signals;

processing applications of the slave apparatus and also processing the binary information received by the sending/receiving circuit; and

supplying an interruption signal when the sending/receiving circuit has received the start of a new message after the start of the new message has been acknowledged and recorded by the sending/receiving circuit.

21. The method of Claim 20 wherein supplying the interruption signal comprises setting an interruption state latch to a predetermined logic level based upon the status signals to indicate a microprocessor interruption request.

22. A method of processing interruptions in a slave apparatus for communicating with a master apparatus via the universal serial bus (USB) protocol, the method comprising:

generating a state signal indicating the end of a message;

detecting a start of a new message from the master apparatus and producing a start of message state signal;

recording data from the start of the new message;

acknowledging receipt of the start of the new message;

generating a signal indicating completion of recordation of the data from the start of the new message; and

generating an interruption signal in the presence of the state signal indicating the end of the message, the start of message state signal, and the signal indicating completion of recordation of the data from the start of the new message.

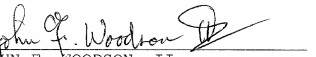
REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability.

Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

In re Patent Application of:
MARIAUD ET AL.
Serial No. **Not yet assigned**
Filed: **Herewith**
_____/

Respectfully submitted,



JOHN F. WOODSON, II
Reg. No. 45,236
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
407-841-2330
407-841-2343 fax
Attorneys for Applicants